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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,234	12/28/2001	Salman Akram	2754.5US (95-0742.5)	9689

24247 7590 08/14/2002

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EXAMINER	
GRAYBILL, DAVID E	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 08/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/033,234	Applicant(s) AKRAM ET AL.	
	Examiner David E Graybill	Art Unit 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 37 and 39 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The non-statutory subject matter is the entire claims, which are drawn to an abstract idea.

In particular, in claims 37 and 39 the conditional limitations, "if said first semiconductor device is determined to be unacceptable," and, "if said second semiconductor device is determined to be unacceptable," respectively, are language that suggests or makes optional but do not require steps to be performed when the conditions introduced by the conditional term "if" are not met; therefore, the limitations do not limit the scope of the claims. See MPEP 2106C.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 12, 13, 16 and 34-41 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to

reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

Specifically, there is no description in the specification for the claim 12 limitation, "the third semiconductor device installed in the at least one other vacant position having said predetermined performance capability," the claim 16, limitation, "said third semiconductor device installed in said at least one other vacant position having said predetermined performance capability of a combined predetermined performance capability of said first and the second semiconductor device," the claim 34 limitation, "said third semiconductor device having a performance capability of said unacceptable semiconductor device," the claim 37 limitation, "said third semiconductor device having a performance capability of said first semiconductor device if said first semiconductor device is determined to be unacceptable," and the claim 39 limitation, "a fourth semiconductor device having a performance capability of said second semiconductor device if said second semiconductor device is determined to be unacceptable."

To further clarify, the specification describes only semiconductor devices having a performance capability not possessed by devices determined to be unacceptable.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 12-41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 21, 22, 25, 27-31 and 34-36 the scope of the limitation "configuration for corresponding to" is unclear because the properties of the configuration that satisfy the intended use criterion "for corresponding to" are not recited, and cannot otherwise be adequately determined.

There is insufficient antecedent basis for the following:

In claims 12 and 13, "the unacceptable semiconductor device";

In claims 14, 17-23, 26, 32-34, 38, 40 and 41, "said unacceptable semiconductor device";

In claim 16, "said predetermined performance capability of a combined predetermined performance capability of said first and the second semiconductor device."

In claim 12, there is ambiguous and insufficient antecedent basis for the language, "said predetermined performance

capability" because there are at least two possible antecedent bases in the phrase "the first and second semiconductor devices each having a predetermined performance capability."

In the rejections infra, reference labels are generally recited only for the first recitation of identical claim language.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 7, 8, 12-15 and 23-41 are rejected under 35 U.S.C. 102(b) as being anticipated by Corbett (4992850).

At column 3, line 31 to column 4, line 36, column 4, lines 63-65, column 5, lines 4-47, column 6, line 1 to column 7, line 66, column 8, lines 16-21, column 8, line 37 to column 9, line 37, and column 9, line 65 to column 10, line 12, Corbett teaches the following:

1. A method of manufacturing a multichip module system comprising: forming a substrate 23 for use in said multichip module system, said substrate having at least a first position ["plurality of die receiving portions"] for locating a first

semiconductor device thereat and having at least one other vacant position ["plurality of die receiving portions"] for locating a second semiconductor device thereat on said substrate; installing said first semiconductor device 31 in the at least a first position of the substrate; determining if the multichip module system has an unacceptable semiconductor device ["functional testing"]; and repairing the substrate ["the failed parts will then be replaced"] to have an acceptable semiconductor device by installing a second semiconductor device ["replacement die 31"] in the at least one other vacant position in the substrate.

2. The method of 1, further comprising: installing a known-good-die in the at least one other vacant position on the substrate for use in said multichip module system.

3. The method of 1, further comprising: testing said multichip module system for compliance with predetermined operational characteristics ["functional testing"] for the second semiconductor device.

7. A method of manufacturing a multichip module system comprising: forming a substrate for use in said multichip module system, the substrate having at least a first position for locating a first semiconductor device thereat and having at least one other vacant position for locating a second

semiconductor device thereat on the substrate; installing said first semiconductor device in the at least a first position of the substrate; determining if the multichip module system has an unacceptable semiconductor device; and repairing the substrate to have an acceptable semiconductor device by installing said second semiconductor device in the at least one other vacant position in the substrate, the second semiconductor device comprising a known-good-die.

8. The method of 7, further comprising: testing said multichip module system to ensure compliance with predetermined operational characteristics for the second semiconductor device.

12. A method of manufacturing a multichip module system comprising: forming a substrate for use in said multichip module system, the substrate having at least first and second positions thereon ["plurality of die receiving portions"], the at least first and second positions for locating a first and second semiconductor device thereat, and having at least one other vacant position ["plurality of die receiving portions"] for locating a third semiconductor device thereat on the substrate; installing said first and second semiconductor devices 31, 31 in the respective at least first and second positions of the substrate, the first and second semiconductor devices each having a predetermined performance capability; determining if

the multichip module system has an unacceptable semiconductor device thereon; disabling circuitry connected to the unacceptable semiconductor device ["removal of the unsupported traces close to the defective die 31"]; and repairing the substrate to have an acceptable semiconductor device thereon by installing a third semiconductor device 31 in the at least one other vacant position in the substrate, the third semiconductor device installed in the at least one other vacant position having said predetermined performance capability.

13. The method of 12, further comprising: removing the unacceptable semiconductor device from the substrate.

14. A method of manufacturing a multichip module system comprising: forming a substrate for use in said multichip module system, said substrate having at least first and second positions for locating a first and second semiconductor device thereat, and having at least one other vacant position for locating a third semiconductor device thereat; installing a first and second semiconductor device in said respective first and second positions of said substrate, said first and second semiconductor devices each having a predetermined performance capability; determining if said multichip module system has an unacceptable semiconductor device thereon; disabling circuitry connected to said unacceptable semiconductor device; and

repairing said substrate to have an acceptable semiconductor device thereon by installing said third semiconductor device in said at least one other vacant position in said substrate, said third semiconductor device installed in said at least one other vacant position having a predetermined performance capability, said third semiconductor device comprising a known-good-die having a predetermined performance capability.

15. The method of 14, further comprising: testing said multichip module system for compliance with said predetermined performance capability ["functional testing"] for said third semiconductor device.

23. A method of manufacturing a multichip module system comprising: forming a substrate for use in said multichip module system, said substrate having at least a first position for a semiconductor device to be located thereat, having a second position having a second mounting for a semiconductor device to be located thereat different than said at least said first position, and having at least one other vacant position for locating a third semiconductor device thereat on said multichip module system; installing a first semiconductor device in said at least said first position of said substrate; determining if said multichip module system has an unacceptable semiconductor device thereon; disabling said circuitry connected to said

unacceptable semiconductor device; and repairing said substrate to have an acceptable semiconductor device thereon by installing a second semiconductor device in said at least one other vacant position in said substrate.

24. The method of 23, further comprising: wherein said third semiconductor device includes a known-good-die in said at least one other vacant position on said substrate for use in said multichip module system.

25. The method as defined in 23, further comprising: configuring said at least one other vacant position located on said substrate to have a predetermined semiconductor mounting configuration for corresponding to a first mounting configuration of said first semiconductor device and for corresponding to said second mounting of said second semiconductor device.

26. The method of 23, further comprising: removing said unacceptable semiconductor device from said substrate.

27. The method of 23, further comprising: configuring said location of said at least one other vacant position located on said substrate such that on one side of said substrate said at least one other vacant position has a predetermined semiconductor mounting configuration for corresponding to said first semiconductor device; and forming on an other side of said

substrate a second vacant position that has a predetermined configuration for corresponding to said second mounting of said second semiconductor device.

28. The method of 23, further comprising: installing a third semiconductor chip in said at least one other vacant location, said third semiconductor chip having a predetermined mounting configuration for corresponding to said first semiconductor device.

29. The method of 23, further comprising: installing a third semiconductor chip in said at least one other vacant location, said third semiconductor chip having a predetermined mounting configuration for corresponding to the second mounting of said second semiconductor device.

30. The method of 27, further comprising: installing a third semiconductor chip in said at least one other vacant location on said one side of said substrate, said third semiconductor chip having said predetermined mounting configuration for corresponding to said first semiconductor device.

31. The method of 27, further comprising: installing a third semiconductor chip in said second vacant location on said other side of said substrate, said third semiconductor chip having a predetermined mounting configuration for corresponding to said

second mounting configuration of said second semiconductor device.

32. The method of 31, further comprising: disabling circuitry connected to said unacceptable semiconductor device.

33. The method of 31, further comprising: removing said unacceptable semiconductor device from said substrate.

34. A method of manufacturing a multichip module system comprising: forming a substrate for use in said multichip module system, said substrate having at least a first position for locating a semiconductor device thereat, having a second position having a second mounting configuration for locating a semiconductor device thereat different than said at least said first position, having at least a first vacant position having, in turn, a third configuration for locating a third semiconductor device thereat on said substrate, and having a second vacant position having, in turn, a fourth configuration for locating a fourth semiconductor device thereat on said substrate; installing a first semiconductor device in said at least said first position of said substrate, said first semiconductor device having a first performance capability; installing a second semiconductor device in said second position of said substrate, said second semiconductor device having a second performance capability; determining if said multichip

module system contains an unacceptable semiconductor device thereon; determining if said unacceptable semiconductor device is said first semiconductor device; configuring said at least said first vacant position located on said substrate to have a third semiconductor mounting configuration for corresponding to said at least said first position of said first semiconductor device; configuring said second vacant position located on said substrate to have a fourth semiconductor configuration for corresponding to said second mounting configuration of said second semiconductor device; and installing said third semiconductor device having a performance capability of said unacceptable semiconductor device in one of said at least said first vacant position or said second vacant position.

35. The method of 34, further comprising: configuring said second vacant position located on said substrate to have a fourth predetermined semiconductor configuration for corresponding to said second mounting configuration of said second semiconductor device.

36. The method of 34, further comprising: configuring said location of said at least said first vacant position to be located on said substrate on one side thereof such that said one side of said substrate has said at least said first vacant position thereon having a third predetermined semiconductor

mounting configuration for corresponding to a first predetermined mounting configuration of said first semiconductor device; and configuring said location of said second vacant position to be located on an other side of said substrate such that said second vacant position has a fourth predetermined configuration for corresponding to said second mounting configuration of said second semiconductor device.

37. The method of 34, further comprising: installing said third semiconductor device having a performance capability of said first semiconductor device if said first semiconductor device is determined to be unacceptable.

38. The method of 34, further comprising: determining if said unacceptable semiconductor device is said second semiconductor device.

39. The method of 38, further comprising: installing a fourth semiconductor device 31 having a performance capability of said second semiconductor device if said second semiconductor device is determined to be unacceptable.

40. The method of 34, further comprising: removing said unacceptable semiconductor device from said substrate.

41. The method of 34, further comprising: disabling circuitry connected to said unacceptable semiconductor device.

To further clarify the teaching of vacant positions and installing semiconductor dice in the vacant positions, as cited, Corbett teaches removing defective dice, thereby creating vacant positions, and installing replacement dice in the vacant positions.

To further clarify the teaching of mounting configurations "for corresponding to" mounting configurations, these limitations are merely statements of intended purpose which do not result in a manipulative difference as compared to the process of Corbett. Furthermore, because the process of Corbett is inherently capable of being used for the same intended purpose, the statement of intended purpose does not patentably distinguish the claimed process from the process of Corbett.

To further clarify the teaching of configuring said location of said one other vacant position located on said substrate such that on one side of said substrate said one other vacant position has said predetermined semiconductor mounting configuration which corresponds to said first mounting configuration of said first semiconductor device, it is noted that when the first semiconductor located on one side of the substrate is defective and removed, on one side of the substrate the one other vacant position created by the removed first semiconductor device has the predetermined semiconductor

mounting configuration which corresponds to the first mounting configuration of the first semiconductor device.

To further clarify the teaching of forming on an other side of said substrate a second vacant position, as cited, Corbett teaches forming semiconductor devices on an other side, and when a semiconductor located on the other side of the substrate is defective and removed, a second vacant position is formed.

To further clarify the teaching of installing known-good-die, Corbett teaches installing replacement dice that have been "burn-in and the post burn-in functional, speed, and performance" tested; hence the tested replacement die is a known-good-die.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered

therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 4-6, 9-11 and 17-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Corbett as applied to claims 1-3, 7, 8, 12-15 and 23-41, and further in combination with Derouiche (5623395).

As cited, Corbett teaches the following:

4. The method as defined in 1, further comprising: repairing the substrate for use in said multichip module system to have said acceptable semiconductor device thereon by installing said second semiconductor device.

5. The method of 4, further comprising: installing a known-good-die.

6. The method as defined in 5, further comprising: testing said multichip module system to ensure compliance with predetermined operational characteristics for the second semiconductor device.

9. A method of manufacturing a multichip module system comprising: forming a substrate for use in said multichip module

system, the substrate having at least a first position for locating a first semiconductor device thereat and having at least one other vacant position for locating a second semiconductor device thereat on the substrate; installing said first semiconductor device in the at least a first position of the substrate; determining if the multichip module system has an unacceptable semiconductor device; and repairing the substrate to have an acceptable semiconductor device thereon by installing said second semiconductor device.

10. The method of 9, further comprising: installing a known-good-die.

11. The method as defined in 10, further comprising: testing said multichip module system for compliance with predetermined operational characteristics for the second semiconductor device.

17. A method of manufacturing a multichip module system comprising: forming a substrate for use in said multichip module system, said substrate having at least first and second positions thereon, said first and second positions each for locating a first and second semiconductor device thereat, and having at least one other vacant position for locating a third semiconductor device thereat on said substrate; installing a first and second semiconductor device in said respective first and second positions of said substrate, said first and second

semiconductor devices each having a predetermined performance capability; determining if said multichip module system has an unacceptable semiconductor device thereon; disabling circuitry connected to said unacceptable semiconductor device; and repairing said substrate to have an acceptable semiconductor device thereon by installing said third semiconductor device.

18. The method of 17, further comprising: installing a known-good-die as said third semiconductor device.

19. The method as defined in 18, further comprising: testing said multichip module system for compliance of said third semiconductor device with a predetermined performance capability for said third semiconductor device.

20. The method of 17, further comprising: forming said substrate for use in said multichip module system, said substrate having at least a first position having a first mounting configuration for a semiconductor device thereat, having a second position having a second mounting configuration for a semiconductor device thereat different than said first mounting configuration, and having said at least one other vacant position having, in turn, a predetermined configuration for locating said third semiconductor device thereat on said multichip module system.

21. The method of 20, further comprising: configuring one other vacant position located on said substrate to have a

predetermined semiconductor mounting configuration for corresponding to said first mounting configuration of said first semiconductor device and for corresponding to said second mounting configuration of said second semiconductor device.

22. The method of 21, further comprising: configuring said location of said one other vacant position located on said substrate such that on one side of said substrate said one other vacant position has said predetermined semiconductor mounting configuration which corresponds to said first mounting configuration of said first semiconductor device; and forming on an other side ["separate from said one side"] of said substrate a second vacant position that has a predetermined configuration for corresponding to said second mounting configuration of said second semiconductor device.

However, Corbett does not appear to explicitly teach installing said second semiconductor device having an adapter attached thereto, the adapter having to be operably installed in the at least one other vacant position in the substrate; installing a known-good-die having said adapter attached thereto, the adapter to be operably installed in the at least one other vacant position in the substrate for use in said multichip module system as the second semiconductor device;

installing said third semiconductor device having an adapter attached thereto, said adapter for installation in said at least one other vacant position in said substrate; and installing a known-good-die as said third semiconductor device having said adapter attached thereto, said adapter for installation in said at least one other vacant position in said substrate for use in said multichip module system as said third semiconductor device.

Regardless, at column 4, lines 16-36, Derouiche teaches installing a semiconductor device 30a having an adapter 42 attached thereto, the adapter having to be operably installed in a vacant position in a substrate for use in a multichip module system as the second semiconductor device.

Furthermore, it would have been obvious to combine the process of Derouiche with the process of Corbett because it would facilitate connection of a semiconductor device to the substrate of Corbett.

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a

terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claims 1-41 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-41 of prior U.S. Patent No. 6,345,565. This is a double patenting rejection.

To further clarify, although some of the instant claims are differently worded than claims of the prior patent, they define the same invention. Specifically, the claims of the prior patent recite various "configuration" limitations not recited by the instant claims. However, the instant claims define the same invention as the prior patent claims because the various "configuration" limitations are inherent properties of the process of the instant claims. Also, the remaining grammar of the claims of the prior patent differs slightly from that of the instant claims, but the differences are not semantically significant, and the scope of the instant claims is the same as the scope of the prior patent claims.

Claims 1-34 and 36-41 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-40 of prior U.S. Patent No. 5,807,762. This is a double patenting rejection.

To further clarify, although some of the instant claims are differently worded than claims of the prior patent, they define the same invention. Specifically, the grammar of the claims of

the prior patent differs slightly from that of the instant claims, but the differences are not semantically significant, and the scope of the instant claims 1-34 and 36-41 is the same as the scope of the prior patent claims 1-40.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Customer Service whose telephone number is 703-306-3329.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is 703/3087724.

David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
8-Aug-02